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A Transformer-Less Adaptable Voltage Quadrupler DC Boost Converter with PI Controller

R.Latha[1*], B.Gayathri Devi [2]

[1,2] *Electrical and Electronics Engineering, Mookambigai College of Engineering, India.*

[*]Corresponding author

Abstract

In this paper, a transformer-less adaptable voltage quadrupler dc boost converter with PI controller to enhance high-voltage transfer gain and reduced semiconductor voltage stress is proposed. The proposed topology utilizes input-parallel output-series configuration for providing a much higher voltage gain without adopting an extreme large duty cycle. The proposed converter cannot only achieve high step-up voltage gain with reduced number of component. It also reduce the voltage stress of both active switches and diodes. This will allow to choose lower voltage rating of MOSFETs and diodes to reduce both switching and conduction losses. Closed loop PI controller is used to achieve the desired output voltage.

The operation principle, steady analysis, driving scheme are presented. Finally, some simulation and experimental results are also presented to demonstrate the effectiveness of the proposed converter.

Keywords: Transformer-Less, Boost Converter, PI Controller, MOSFET.

1. Introduction

For Global energy shortage a renewable energy sources such as solar cells and fuel cells are increasingly widely used. However, due to the inherent low voltage characteristic of these sources, a high step-up dc converter is essential as a pre stage of the corresponding power conditioner. In this paper, a transformer-less adaptable voltage quadrupler dc boost converter with PI controller topology is proposed. It integrates two-phase interleaved boost converter to realize a high voltage gain and maintain the advantage of an automatic current sharing capability simultaneously. Furthermore, the voltage stress of active switches and diodes in the proposed converter can be greatly reduced to enhance overall conversion efficiency. First, the circuit topology and operation principle are given in Section IV. Then, the corresponding steady-state analysis is made in Section VI to provide some basic converter characteristics. A prototype is then constructed and some simulation and experimental results are then presented in Section VII and VIII for demonstrating the merits and validity of the proposed converter. Finally, some conclusions are offered in the last section.

2. Existing System

The conventional boost and buck-boost converters, due to the degradation in the overall efficiency as the duty ratio approaches unity. Besides, the extreme duty ratio not only induces very large spikes and increases conduction losses but also induces severe diode reverse – recovery problem. Active switch of high step-up voltage gain will suffer a high voltage stress due to leakage inductance of the transformer. Output diode voltage stress is much higher than the output voltage, which will degrade the circuit efficiency in the high output voltage applications. Cost is increased because extra power components and isolated sensors or feedback controllers are required.

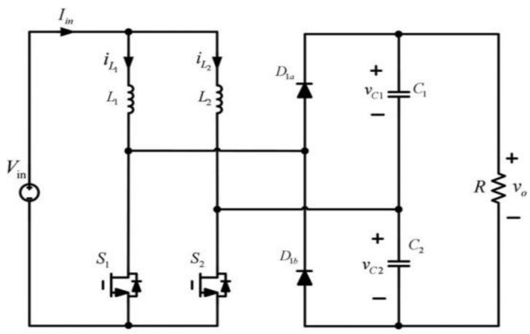

Figure. 1. Configurations of Existing System

Disadvantages of Existing System

- Active switch suffer high voltage stress due to leakage induction of Transformer.
- To achieve High step up gain by increasing the turns ratio of Transformer.
- Very large voltage spikes increases the conduction losses but also induces severe diode reverse recovery problem.
- Input current ripple is relatively high.

- Higher input current ripple will reduce the maximum output power and shorten the usage life of input electrolytic capacitor.
- Higher output voltage stress will degrade the circuit efficiency.
- Cost is high due to extra power components.

3. Proposed System

- With Global energy shortage and strong environmental movements, renewable or clean energy sources such as solar cells and fuel cells are increasingly valued worldwide.

- However due to the inherent low voltage characteristic of these sources, , A Ttransformer-less adaptable voltage quadrupler dc boost converter with PI controller with low switch voltage stress to enhance efficiency has been proposed.

- The proposed topology utilizes input-parallel output-series configuration for providing a much higher voltage gain without adopting an extreme large duty cycle.

- The proposed converter cannot only achieve high step up voltage gain with reduced component count but also reduce the voltage stress of both active switches and diodes.

- This will allow to choose lower voltage rating MOSFETs and Diodes to reduce both switching and conduction losses.

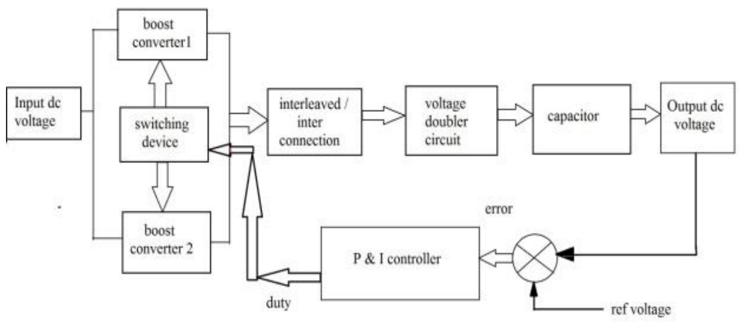

Figure. 2. Block diagram of Proposed system

4. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

The proposed converter topology is basically derived from a two-phase interleaved boost converter and is shown in Fig. 3. Comparing Fig. 1 with Fig. 3, one can see that two more capacitors and two more diodes are added so that during the energy transfer period partial inductor stored energy is stored in one capacitor and partial inductor stored energy together with the other capacitor store energy is transferred to the output to achieve much higher voltage gain. However, the proposed voltage gain is twice that of the interleaved two-phase boost converter. Also, the voltage stress of both active switches and diodes are much lower than the latter. Furthermore, as will be obvious latter, the proposed converter possesses automatic uniform current sharing capability without adding extra circuitry or complex control methods. The detailed operating principle can be illustrated as follows.

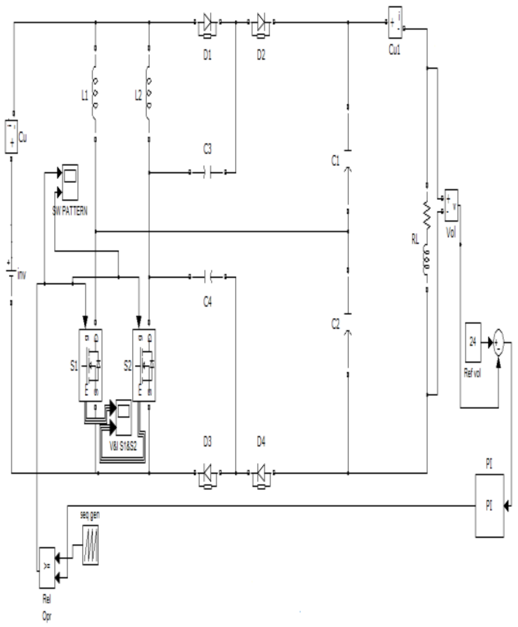

Figure. 3. Circuit diagram of Proposed system

The proposed converter topology, like any existing high step-up dc converter, possesses the drawback of existence of pulsating output period. Furthermore, as the main objective is to obtain high voltage gain and such characteristic can only be achieved when the duty cycle is greater than 0.5 and in continuous conduction mode (CCM); hence, the steady-state

analysis is made only for this case. However, with duty cycle lower than 0.5 or in DCM, as there is no enough energy transfer from the inductors to the blocking capacitors, output capacitors, and load side, and consequently it is not possible to get the high voltage gain as that for duty ratio greater than 0.5. In addition, only with duty cycle larger than 0.5, due to the charge balance of the blocking capacitor, the converter can feature the automatic current sharing characteristic that can obviate any extra current-sharing control circuit. On the other hand, when duty cycle is smaller than 0.5, the converter does not possess the automatic current sharing capability any more,and the current-sharing control between each phases should be taken into a account in this condition.

In order to simplify the circuit analysis of the proposed converter, some assumes are made as follows:

1) All components are ideal components
2) The capacitors are sufficiently large, such that the voltages across them can be considered as constant approximately.
3) The system is under steady state and is operating in CCM and with duty ratio being greater than 0.5 for high step-up

Basically, the operating principle of the proposed converter can be classified into four operation modes. The interleaved gating signals with a 180 phase shift as well as some key operating waveforms are shown in Fig. 7.

4.1. Mode 1 ($t0 \leq t<t1$)

For mode 1, switches S1 and S2 are turned ON, D1a,D1b,D2a,D2b are all OFF. The corresponding equivalent circuit is shown in Fig. 4. From Fig.4, it is seen that both iL1 and iL2 are increasing to store energy in L1 and L2, respectively. The voltages across diodes D1a and D2a are clamped to capacitor voltage VCA and VCB, respectively, and the voltages across the diodes D1b and D2b are clamped to VC 2 minus VCB and VC 1 minus VCA, respectively. Also, the load power is supplied from capacitors C1 and C2. The corresponding state equations are given as follows:

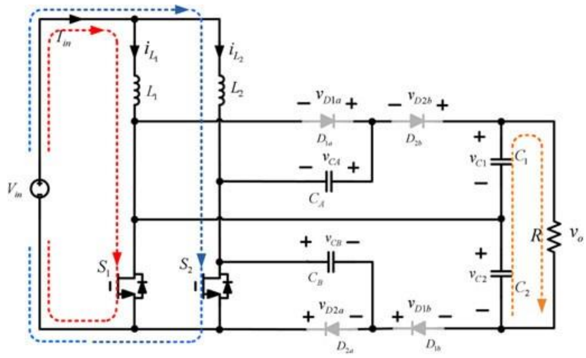

Figure. 4. Mode I

& III Operation

$$C_A \frac{dv_{C_A}}{dt} = 0$$

$$C_B \frac{dv_{C_B}}{dt} = 0$$

$$C_1 \frac{dv_{C_1}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R}$$

$$C_2 \frac{dv_{C_2}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R}$$

b.Mode 2 ($t_1 \le t < t_2$) :

For this operation mode, switch S_1 remains conducting and S_2 is turned OFF. Diodes D_{2a} and D_{2b} become conducting. The corresponding equivalent circuit. It is seen from that part of stored Energy in inductor L_2 as well as the stored energy of C_A is now released to output capacitor C_1 and load. Meanwhile, part of stored energy in inductor L_2 is stored in C_B. In this mode, capacitor voltage V_{C1} is equal to V_{CB} plus V_{CA}. Thus, i_{L1} still increases continuously and i_{L2} decreases linearly. The corresponding state equations are given as follows:

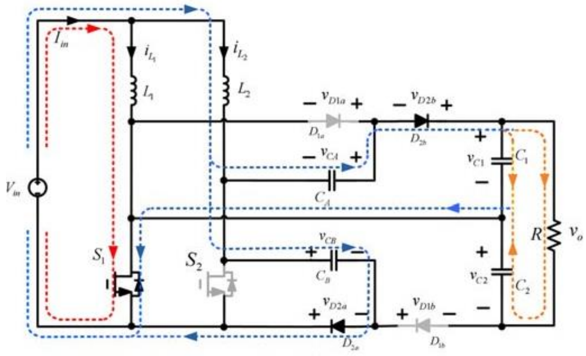

Fig.5: Mode II Operation

$$L_2\frac{di_{L2}}{dt} = V_{\text{in}} + v_{C_A} - v_{C_1} = V_{\text{in}} - v_{C_B}$$

$$C_A\frac{dv_{C_A}}{dt} = i_{C_B} - i_{L_2} \qquad C_B\frac{dv_{C_B}}{dt} = i_{C_A} + i_{L_2}$$

$$C_1\frac{dv_{C_1}}{dt} = -i_{C_A} - \frac{(v_{C_1} + v_{C_2})}{R}$$

$$C_2\frac{dv_{C_2}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R}.$$

c.Mode 3 ($t_2 \leq t < t_3$):

For this operation mode, as can be observed, both S_1 and S_2 are turned ON. The corresponding equivalent circuit turns out to be the same.

d.Mode 4 ($t_3 \leq t < t_4$) :

For this operation mode, switch S_2 remains conducting and S_1 is turned OFF. Diodes D_{1a} and D_{1b} become conducting. The corresponding equivalent circuit. It is seen from that the part of stored energy in inductor L_1 as well as the stored energy of C_B is now released to output capacitor C_2 and load. Meanwhile, part of stored energy in inductor L_1 is stored in C_A. In this mode, the output capacitor voltage V_{C2} is equal to V_{CB} plus V_{CA}. Thus, i_{L2} still increases continuously and i_{L1} decreases linearly. The corresponding state equations are given as follows:

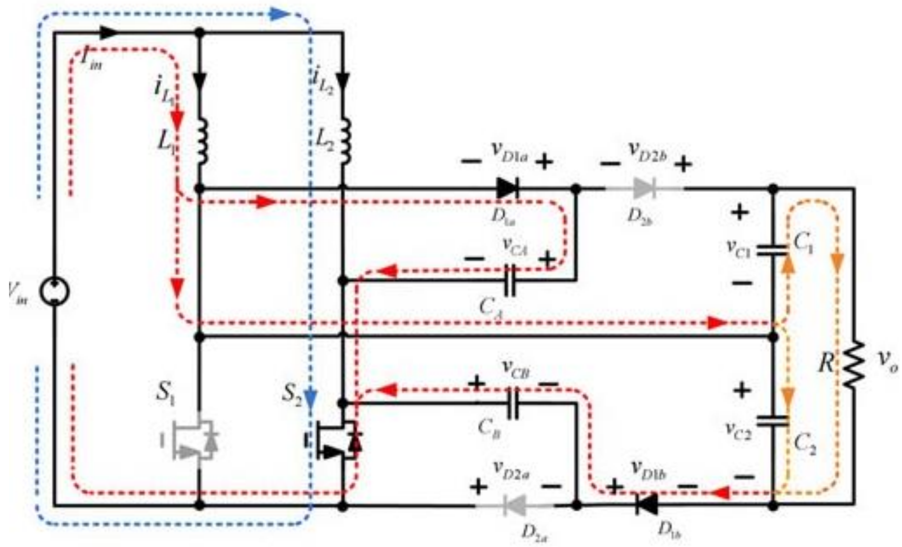

Figure. 6. Mode IV Operation

$$L_1 \frac{di_{L1}}{dt} = V_{\text{in}} - v_{C_2} + v_{C_B} = V_{\text{in}} - v_{C_A}$$

$$C_A \frac{dv_{C_A}}{dt} = i_{C_B} + i_{L_1}$$

$$C_B \frac{dv_{C_B}}{dt} = i_{C_A} - i_{L_1}$$

$$C_1 \frac{dv_{C_1}}{dt} = -\frac{(v_{C_1} + v_{C_2})}{R}$$

$$C_2 \frac{dv_{C_2}}{dt} = -i_{C_B} - \frac{(v_{C_1} + v_{C_2})}{R}$$

5. Driving Scheme

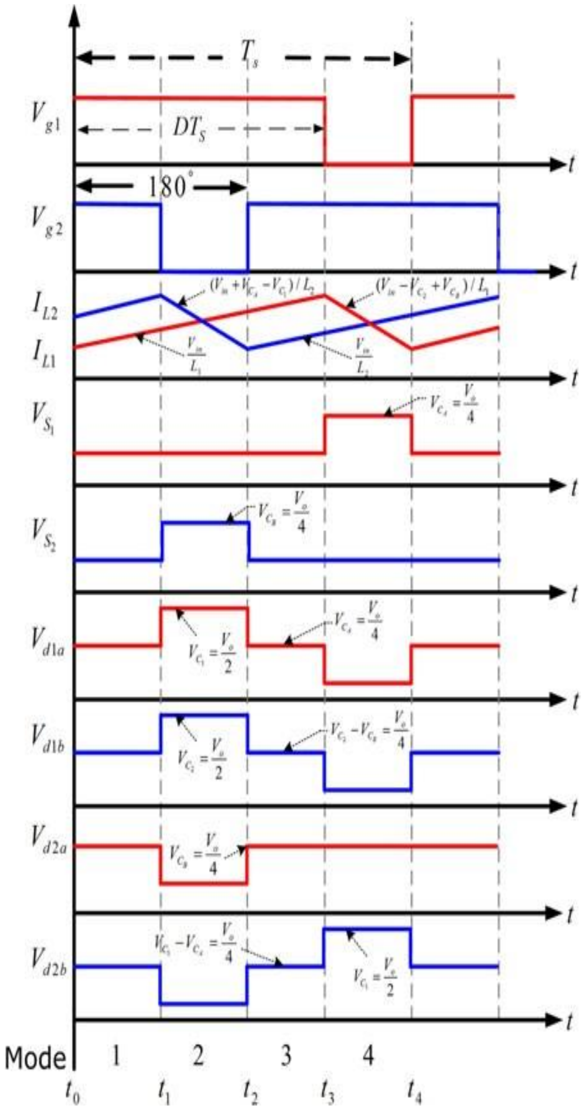

Figure. 7. Driving Signal Key Waveforms

6. STEADY-STATE ANALYSIS

In order to simplify the circuit performance analysis of the proposed converter in CCM, the same assumptions made in the previous section will be adopted.

a.VOLTAGE GAIN

The volt–second relationship of inductor L_1 (or L_2), one can obtain the following relations:

$$V_{in}D + (V_{in} - V_{CA})(1 - D) = 0 \quad \text{---- (3.15)}$$

$$V_{in}D + (V_{in} - V_{CB})(1 - D) = 0 \quad \text{---- (3.16)}$$

$$V_{C1} = V_{CA} + V_{CB} = \frac{2}{1-D}V$$

$$V_{C2} = V_{CA} + V_{CB} = \frac{2}{1-D}V_{in}$$

the output voltage can be obtained as follows:

$Vo = VC1 + VC2 = V\text{in}(1 - D)$

Thus, the voltage conversion ratio M of the proposed converter can be obtained as follows:

$$M = \frac{V_o}{V_{\text{in}}} = \frac{4}{1-D}$$

b.Voltage Stresses on Semiconductor Components

To simplify the voltage stress analyses of the components of the proposed converter, the voltage ripples on the capacitors are ignored. one can see that the voltage stresses on active power switches S_1 and S_2 can be obtained directly as shown in the following equation:

$$V_{S1,\max} = V_{S2,\max} = \frac{1}{1-D} V_{\text{in}}$$

Substituting, the voltage stresses on the active power switches can be expressed as

$$V_{S1,\max} = V_{S2,\max} = \frac{V_O}{4}$$

From, one can see that the voltage stress of active switches of the proposed converter is equal to one fourth of the output voltage. Hence, the proposed converter enables one to adopt lower voltage rating devices to further reduce both switching and conduction losses.

As can be observed from the equivalent circuits, the open circuit voltage stress of diodes D_{1a}, $D2a$, $D1b$, and D_{2b} can be obtained.

$$V_{D1a,\max} = V_{D1b,\max} = V_{D2b,\max} = \frac{V_O}{2}, V_{D2a,\max} = \frac{V_O}{4}.$$

In fact, one can see from that the maximum resulting voltage stress of diodes is equal to $V_O/2$. Hence, the proposed converter enables one to adopt lower voltage rating diodes to further reduce conduction losses.

7. Simulation Result

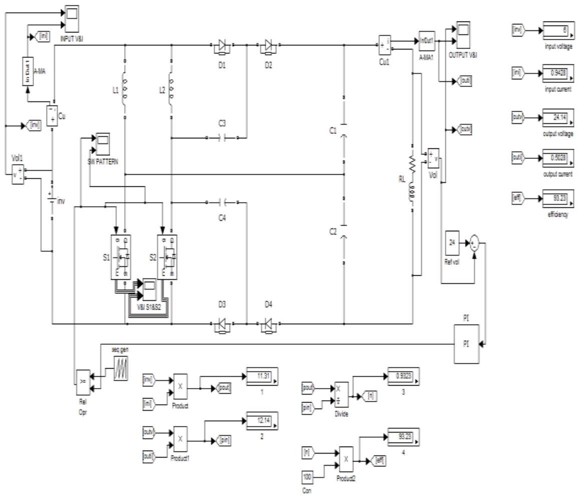

Figure.8. Simulation Circuit diagram

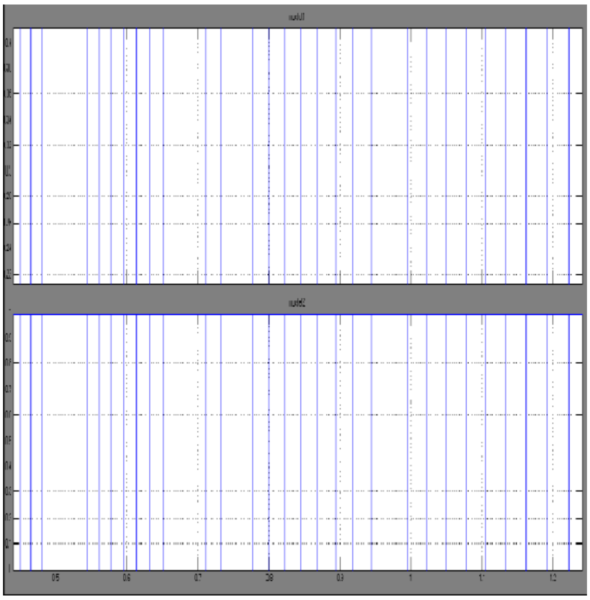

Figure.9. Pwm For Mosfet1&2 (Input Pulses)

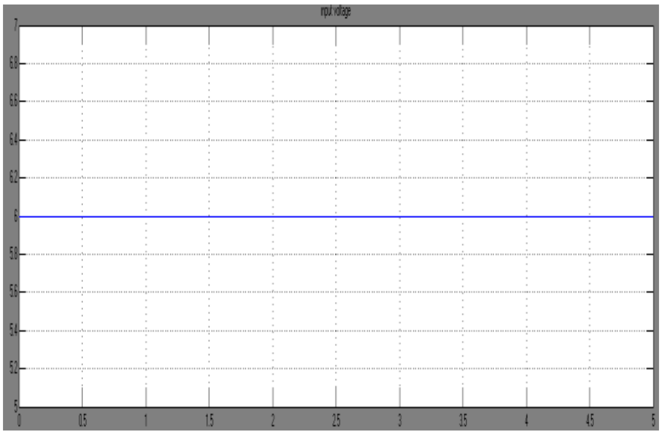

Figure.10. Input Voltage

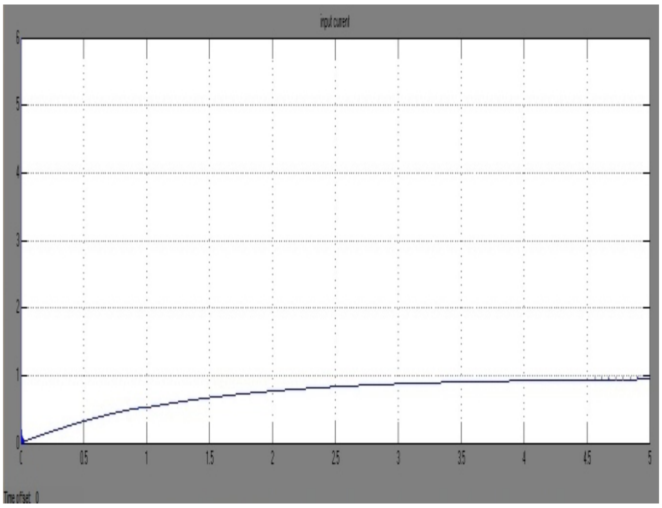

Figure.10. Input Current

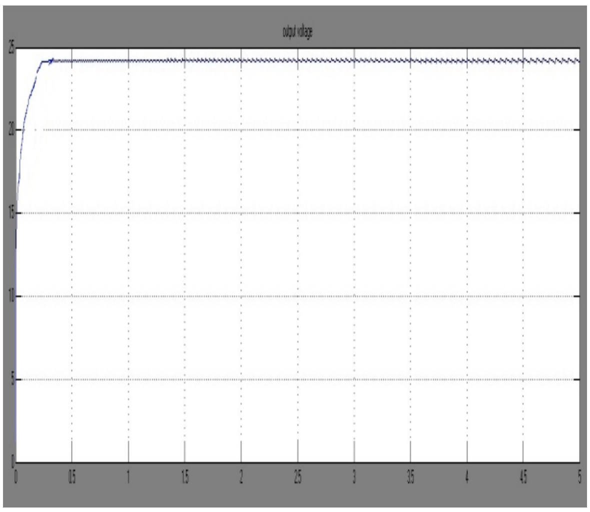

Figure. 12. Output Voltage

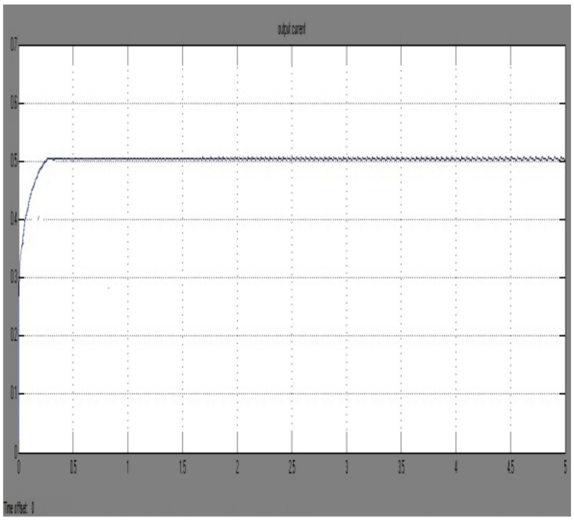

Figure. 13. Output Current

8. Experimental Result

A Transformer-less Adaptable Voltage Quadrupler DC Boost converter with PI Controller prototype is built to verify the circuit operation. The circuit parameters are:

- Input voltage: 12 DC
- Output voltage: 196 DC
- Switching frequency, 100 kHz.

Voltage Gain:

$V_{IN} = 6V$

$V_O = V_{C1}+V_{C2} = \frac{4}{1-??} * V_{IN} = \frac{4}{1-0.75} * 6 = 96$

$V_{C1} = V_{CA}+V_{CB} = \frac{2}{1-??} * V_{IN} = \frac{2}{1-0.75} * 6 = 48$

$V_{C2} = V_{CA}+V_{CB} = \frac{2}{1-??} * V_{IN} = \frac{2}{1-0.75} * 6 = 48$

$V_O = 96V$

8.1. Efficiency

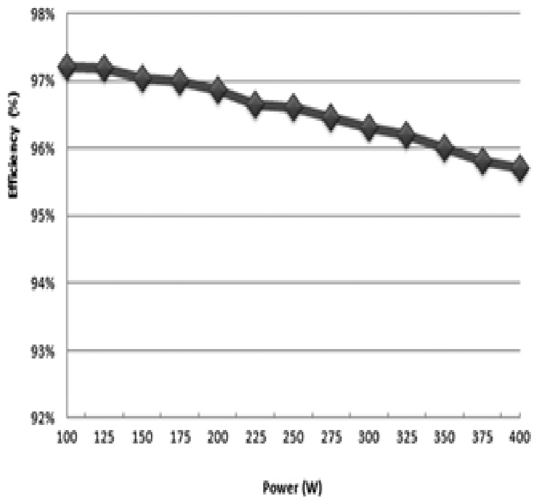

Figure. 14. Efficiency Under Different Load/Source Conditions

9. Conclusion and Future Enhancement

In this paper, A Transformer-less Adaptable voltage Quadrupler DC Boost converter with PI Controller to enhance efficiency with high voltage transfer gain and reduced semiconductor voltage stress is proposed. The proposed topology utilizes input-parallel output-series configuration and is derived from a two-phase interleaved boost converter for providing a much higher voltage gain without adopting an extreme large duty cycle. The proposed converter cannot only achieve high step-up voltage gain but also reduce the voltage stress of both active switches and diodes. This will allow one to choose lower voltage rating MOSFETs and diodes to reduce both switching and conduction losses. Finally, Switching frequency 100 kHz prototype with 12-V input and 196-V output is constructed for verifying the validity of the proposed converter. It is seen that the resulting experimental results indeed agree very close and show great agreement with the simulation results. Therefore, the proposed converter is very suitable for applications requiring high step-up voltage gain.

According to the Project, the required components will be purchased and tested..Followed by that the circuit board will be designed and tested to be done accordingly. After the completion of the above task the microcontroller board will be designed and debugged. Hardware implementation can be done in future.

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